

REMARKS


This application is a divisional application. Claims 5 and 6 have been editorially amended. Claims 15-17 are added. Further, the specification was amended to place the claims on a separate page, pursuant to 37 C.F.R. § 1.75(h).

In the first Preliminary Amendment, dated December 21, 2001, at the top of page 5 and again on page 10, an amendment to claim 10 was inadvertently marked as being an amendment to claim 5. The remarks in the amendment refer to an amendment to claim 10. Claim 5 *was not* amended in the first Preliminary Amendment of December 21, 2001.

The attachment to this Amendment entitled "**Version with Markings to Show Changes Made**" is a marked-up version of the changes made to the claims. The pending claims correspond to Group II, as set forth in the Restriction mailed December 4, 2000 in the parent application, U.S. Patent Application No. 09/663,692, filed September 19, 2000. Applicant hereby requests an action on the merits at the earliest opportunity for claims 5-17 corresponding to Group II.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

5. (Amended) A method of manufacturing a semiconductor electronic device, comprising the following steps:

a step for forming a gate electrode of a field effect transistor over a substrate;

a step for forming first side walls over side walls of said gate electrode on a self-alignment basis respectively;

a step for performing over etching and etching edges of said first side walls ~~until the~~ exposure of said substrate by using trenching effects at the edges of said first side walls until said substrate is exposed;

a step for subjecting the exposed substrate to thermal oxidation to thereby form an oxide film substantially identical in quality to a gate oxide film; and

a step for forming second side walls over side walls of said first side walls; and wherein said respective steps are successively executed.

6. (Amended) A method of manufacturing a semiconductor electronic device, comprising the following steps:

a step for forming a gate electrode of a field effect transistor over a substrate;

a step for forming first side walls over side walls of said gate electrode on a self-alignment basis respectively;

a step for performing over etching and etching edges of said first side walls ~~until the~~
exposure of said substrate by using trenching effects at the edges of said first side walls until said
substrate is exposed;

a step for further etching said exposed substrate;

a step for forming an oxide film on said exposed substrate substantially identical in
quality to a gate oxide film by thermal oxidation; and

a step for forming second side walls over side walls of said first side walls;

and wherein said respective steps are successively executed.

10. (Previously Amended) The method as claimed in claims 5-9, wherein said
substrate is an SOI substrate or an Si substrate.

invention, will be apparent to those skilled in the art
on reference to this description. It is therefore
contemplated that the appended claims will cover any
such modifications or embodiments as fall within the
5 true scope of the invention.